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09/751,377	12/29/2000	Anthony X. Jarvis	00-BN-055 (STMI01-00055)	8283

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,377	JARVIS, ANTHONY X.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6-14, and 16-22 have been examined. Claims 5 and 15 have been cancelled as per Applicant's request.

2. In view of the Appeal Brief filed on 28 October 2004, PROSECUTION IS HEREBY REOPENED. Please see the rejection set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

4. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Papers Submitted

5. It is hereby acknowledged that the following papers have been received and placed on record in the file: Notice of Appeal as filed on 24 August 2004; One Month Extension of Time as filed on 24 August 2004; and Appeal Brief filed 28 October 2004.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 6-10, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi, U.S. Patent No. 5,805,852 (herein referred to as Nakanishi) in view of Barry et al., U.S. Patent Number 6,167,501 (herein referred to as Barry).

8. Regarding claim 1, Nakanishi has taught a data processor comprising:

a. An instruction execution pipeline comprising:

i. A read stage (Nakanishi "MEM" stage, see Col.9 lines 13-23),

ii. A write stage (Nakanishi "WB" stage, see Col.9 lines 13-23),

iii. A first execution stage (Nakanishi "EX" stage, see Col.9 lines 13-23) comprising E execution units capable of producing data results from data operands (Nakanishi "EX" stages of 7-1 through 7-4 of Fig.1, and Col.10 lines 1-5),

b. A register file (Nakanishi 5 of Fig.1) comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline (Nakanishi Col.9 lines 53-56) via at least one of R read ports of said register file (Nakanishi Col.9 lines 5-9) and each of said data registers capable of being written by said write stage of said instruction pipeline (Nakanishi Col.9 lines 61-64) via at least one of W write ports of said register file (Nakanishi Col.9 lines 5-9),

c. Bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising a first plurality of bypass tri-state line drivers having input channels coupled to first output channels of a first plurality of said source

devices and tri-state output channels coupled to a first common read data channel in said read stage (Nakanishi Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

9. Nakanishi has not taught a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage. Barry has taught a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized that the multiplexer, also known as switches, of Barry supports multiple communication patterns while lowering implementation costs (Barry column 1, lines 22-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiplexer of Barry in the device of Nakanishi to lower implementation costs.

10. Regarding claim 2, Nakanishi has taught the data processor as set forth in claim 1 above, wherein said bypass circuitry further comprises a second plurality of bypass tri-state line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tri-state output channels coupled to a second common read data channel in said read stage (Nakanishi Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

11. Regarding claim 3, Nakanishi has taught the data processor as set forth in claim 2 above, further comprising a first register file tri-state line driver having an input channel coupled to a

first one of said R read ports and an output channel coupled to said first common read data channel in said read stage (Nakanishi Fig.3, and Col.10 lines 48-60).

12. Regarding claim 4, Nakanishi has taught the data processor as set forth in claim 3 above, further comprising a second register file tri-state line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage (Nakanishi Fig.3, and Col.10 lines 48-60).

13. Referring to claims 6-10 and 21, Nakanishi has taught the processing system of claim 1, further comprising a latch (Nakanishi L1-L8 of Fig.3) coupled to the output channel and to the first operand channel of the first execution unit (Nakanishi Col.10 lines 11-60). Nakanishi has not taught

a. A second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (Applicant's claim 6);

b. Wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer (Applicant's claim 7);

c. Wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (Applicant's claim 8);

d. Wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (Applicant's claim 9);

e. Wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (Applicant's claim 10); and

f. A first multiplexer (Applicant's claim 21).

14. Barry has taught

a. A second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (Applicant's claim 6) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

b. Wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer (Applicant's claim 7) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

c. Wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (Applicant's claim 8) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

d. Wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (Applicant's claim 9) (Barry column 7,

lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

e. Wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (Applicant's claim 10) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D); and

f. A first multiplexer (Applicant's claim 21) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D).

15. A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized that the multiplexer, also known as switches, of Barry supports multiple communication patterns while lowering implementation costs (Barry column 1, lines 22-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiplexer of Barry in the device of Nakanishi to lower implementation costs.

16. Claims 11-14, 16-20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi, U.S. Patent No. 5,805,852 (herein referred to as Nakanishi) in view of Barry et al., U.S. Patent Number 6,167,501 (herein referred to as Barry) and in further view of Ferris, III et al., U.S. Patent Number 4,591,973 (herein referred to as Ferris).

17. Regarding claims 11, Nakanishi has taught a processing system comprising:

a. A data processor (Nakanishi Fig.1), wherein said data processor comprises:

i. An instruction execution pipeline comprising:

(1) A read stage (Nakanishi "MEM" stage, see Col.9 lines 13-23),

(2) A write stage (Nakanishi "WB" stage, see Col.9 lines 13-23),

(3) A first execution stage (Nakanishi "EX" stage, see Col.9 lines 13-23) comprising E execution units capable of producing data results from data operands (Nakanishi "EX" stages of 7-1 through 7-4 of Fig.1, and Col.10 lines 1-5),

ii. A register file (Nakanishi 5 of Fig.1) comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline (Nakanishi Col.9 lines 53-56) via at least one of R read ports of said register file (Nakanishi Col.9 lines 5-9) and each of said data registers capable of being written by said write stage of said instruction pipeline (Nakanishi Col.9 lines 61-64) via at least one of W write ports of said register file (Nakanishi Col.9 lines 5-9),

iii. Bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising:

(1) A first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage (Nakanishi Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

b. A memory coupled to said data processor (Nakanishi 1 of Fig.1).

18. Nakanishi has not explicitly taught a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor. Ferris has taught a plurality of memory-mapped peripheral circuits coupled to a data processor (Ferris Fig.1, Col.1 lines 43-52, and Col.3 lines 3-19) in order to decrease the burden on the main processor and provide greater throughput and performance (Ferris Col.1 lines 21-31). One of ordinary skill in the art would have recognized that increasing the performance of microprocessor systems is a primary goal of their designers. Therefore, one of ordinary skill in the art would have found it obvious to modify Nakanishi to include a plurality of memory-mapped peripheral circuits in order to increase the performance of the processor (see Col.1 lines 21-31).

19. In addition, Nakanishi has not taught a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage. Barry has taught a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized that the multiplexer, also known as switches, of Barry supports multiple communication patterns while lowering implementation costs (Barry column 1, lines 22-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiplexer of Barry in the device of Nakanishi to lower implementation costs.

20. Regarding claim 12, Nakanishi in view of Ferris has taught the processing system as set forth in claim 11 above, wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage (see Nakanishi, Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

21. Regarding claim 13, Nakanishi in view of Ferris has taught the processing system as set forth in claim 12 above, further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage (see Nakanishi, Fig.3, and Col.10 lines 48-60).

22. Regarding claim 14, Nakanishi in view of Ferris has taught the processing system as set forth in claim 13 above, further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage (see Nakanishi, Fig.3, and Col.10 lines 48-60).

23. Regarding claims 16-20 and 22, Nakanishi in view of Ferris has taught a latch (Nakanishi, L1-L8 of Fig.3) coupled to the output channel and to the first operand channel of the first execution unit (Nakanishi, Col.10 lines 11-60). Nakanishi in view of Ferris has not taught

a. A second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (Applicant's claim 16);

b. Wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer (Applicant's claim 17);

c. Wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (Applicant's claim 18);

d. Wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (Applicant's claim 19);

e. Wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (Applicant's claim 20); and

f. The first multiplexer (Applicant's claim 22).

24. Barry has taught

a. A second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (Applicant's claim 16) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

b. Wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first

multiplexer (Applicant's claim 17) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

c. Wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (Applicant's claim 18) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

d. Wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (Applicant's claim 19) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D);

e. Wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (Applicant's claim 20) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D); and

f. The first multiplexer (Applicant's claim 22) (Barry column 7, lines 8-19 and 33-46; column 7, line 60 to column 8, line 9; Figure 1D; and Figure 8D).

25. A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized that the multiplexer, also known as switches, of Barry supports multiple communication patterns while lowering implementation costs (Barry column 1, lines 22-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time

the invention was made to incorporate the multiplexer of Barry in the device of Nakanishi to lower implementation costs.

Response to Arguments

26. Applicant's arguments, see Appeal Brief, filed 28 October 2004, with respect to the rejection(s)of claim(s) 1-4, 6-14, and 16-22 under Nakanishi, U.S. Patent Number 5,805,852, and Nakanishi in view of Ferris, III et al., U.S. Patent Number 4,591,973, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Mehra, U.S. Patent Number 5,974,537, has taught a multiplexer selecting data being fed into an execution unit.

b. Dowling, U.S. Patent Number 6,170,051, has taught a multiplexer selecting data being fed into an execution unit.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
5 January 2005

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